Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

24. (Allowed) A semiconductor device formed by the method comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged by implantation monocrystalline semiconductor material below said selected depth comprising a second layer of the undamaged by implantation monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a first layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

forming a semiconductor device on said second layer of undamaged by implantation monocrystalline semiconductor material or on layer of epitaxial monocrystalline semiconductor material deposited on said second layer; and

wherein the said semiconductor device is formed on said epitaxial layer.

25. (Allowed) The semiconductor device of claim 24 wherein said device is selected form the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resistor, a thyristor and combinations thereof comprising integrated circuits.

26. (Allowed) Currently amended) A semiconductor device formed by the process comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged by implantation monocrystalline semiconductor material below said selected depth comprising a second layer of the undamaged by implantation monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a first layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth between the first layer of monocrystalline

semiconductor material and the second layer of undamaged by implantation monocrystalline semiconductor material;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer adjacent the first layer of monocrystalline semiconductor material, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions;

wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide; and

forming a semiconductor device on said bonded substrate.

27. (Allowed) The semiconductor device of claim 26 wherein said device is selected from the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resister, a thyristor, and combinations thereof comprising integrated circuits.

28. (Allowed) A bonded semiconductor-on-insulator substrate for semiconductor devices and integrated circuits, said substrate comprising:

a wafer comprising a mononcrystalline semiconductor material and having a first surface and a second surface, said wafer comprising a first layer of the monocystalline semiconductor material adjacent to said first surface and a second layer of undamaged by implantation monocrystalline semiconductor material adjacent to said second surface, and interposed between said first and second layers of the monocrystalline semiconductor material, a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites,

an insulating bond layer disposed on said first surface of said wafer; and

a handle wafer bonded to said insulting bond layer.

29. (Allowed) The substrate of claim 28 wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions.

30. (Allowed) The substrate of claim 28 wherein the monocrystalline semiconductor material comprises silicon and the substantially planer intrinsic gettering zone is formed by implanting ions of silicon through the first layer of monocrystalline semiconductor material.

31. (Allowed) The substrate of claim 28 wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide.

32. (Allowed) The substrate of claim 28 wherein said first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

33. (Allowed) The substrate of claim 28 wherein said second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

34. (Allowed) The substrate of claim 28 wherein said gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

35. (Allowed) The substrate of claim 28 further comprising two or more devices and one or more trenches surrounding at least one of said devices for laterally isolating the surrounded device form the other device(s).

36. (Allowed) A semiconductor device formed on the second layer of monocrystalline semiconductor material of the substrate of claim 28 or on a layer of epitaxial monocrystalline semiconductor material deposited on said second layer.

37. (Allowed) The semiconductor device of claim 36 wherein said device is selected form the group consisting of a bipolar junction transistor, field effect transistor, capacitor, a resistor, a thyristor, and combinations thereof comprising integrated circuits.

38. (Allowed) A bonded semiconductor-on-insulator substrate for an integrated circuit comprising:

a wafer, the wafer having a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer, the wafer further having a second layer of undamaged by implantation monocrystalline semiconductor material adjacent a second surface of the wafer, the wafer further having a substantially planar intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers formed by implanting ions of the semiconductor material through the first layer of monocrystalline semiconductor material;

a handle wafer; and

an insulating bond layer bonding the handle wafer to the first surface of the wafer.

39. (Allowed) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the first and second layers of monocrystalline semiconductor comprises silicon and the ions implanted through the first layer are silicon ions.

40. (Allowed) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the second layer of undamaged monocrystalline semiconductor material is a device layer upon which semiconductor devices are formed.

41. (Allowed)The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the handle wafer comprises silicon and the insulating bond layer comprises silicon dioxide.

42. (Allowed) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

43. (Allowed) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

44. (Allowed) The bonded semiconductor–on-insulator substrate for an integrated circuit of claim 38, wherein the gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

46. (Allowed) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the second layer.

47. (Allowed) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 46, further comprising:

two or more semiconductor devices formed in the epitaxial monocrystalline semiconductor material, wherein the semiconductor devices are laterally isolated form each other.

48. (Allowed) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, further comprising:

two or more semiconductor devices formed in the bonded semiconductor-on-insulator substrate, wherein each semiconductor device is laterally isolated from each other.

49. (Currently Amended) A bipolar junction transistor for an integrated circuit comprising:

a wafer, the wafer having a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer, the wafer further having a second layer of undamaged by implantation monocrystalline semiconductor material adjacent a second surface of the wafer, the wafer further having a substantially ~~planer~~ planar intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers formed by implanting ions of the semiconductor material through the first layer of monocrystalline semiconductor material;

a handle wafer;

an insulating bond layer bonding the handle wafer to the ~~second~~ first surface of the wafer;

a layer of epitaxial monocrystalline semiconductor material deposited on the first layer;

an emitter diffusion formed in the epitaxial monocyrstalline semiconductor material;

a base diffusion formed in the epitaxial monocyrstalline semiconductor material; and

a collector sinker diffusion formed in the epitaxial monocyrstalline semiconductor material, wherein the emitter, base and collector sinker diffusions are laterally isolated from other devices formed in the epitaxial monocyrstalline semiconductor material of the integrated circuit.

50. (Previously Presented)The bipolar junction transistor for an integrated circuit of claim 49, wherein the first and second monocrystalline semiconductor material comprises silicon implanted by silicon ions.

51. (Previously Presented)The bipolar junction transistor for an integrated circuit of claim 49, further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the second layer of monocrystalline semiconductor material.

52. (Previously Presented)The bipolar junction transistor for an integrated circuit of claim 49, wherein the handle wafer comprises silicon and the insulating bond layer comprises silicon dioxide.

53. (Previously Presented)The bipolar junction transistor for an integrated circuit of claim 49, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

54. (Previously Presented)The bipolar junction transistor for an integrated circuit of claim 49, wherein the second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

55. (Previously Presented)The bipolar junction transistor for an integrated circuit of claim 49, wherein the gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

56. (Previously Presented)The bipolar junction transistor for an integrated circuit of claim 49, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.